Data Conversion Fundamentals

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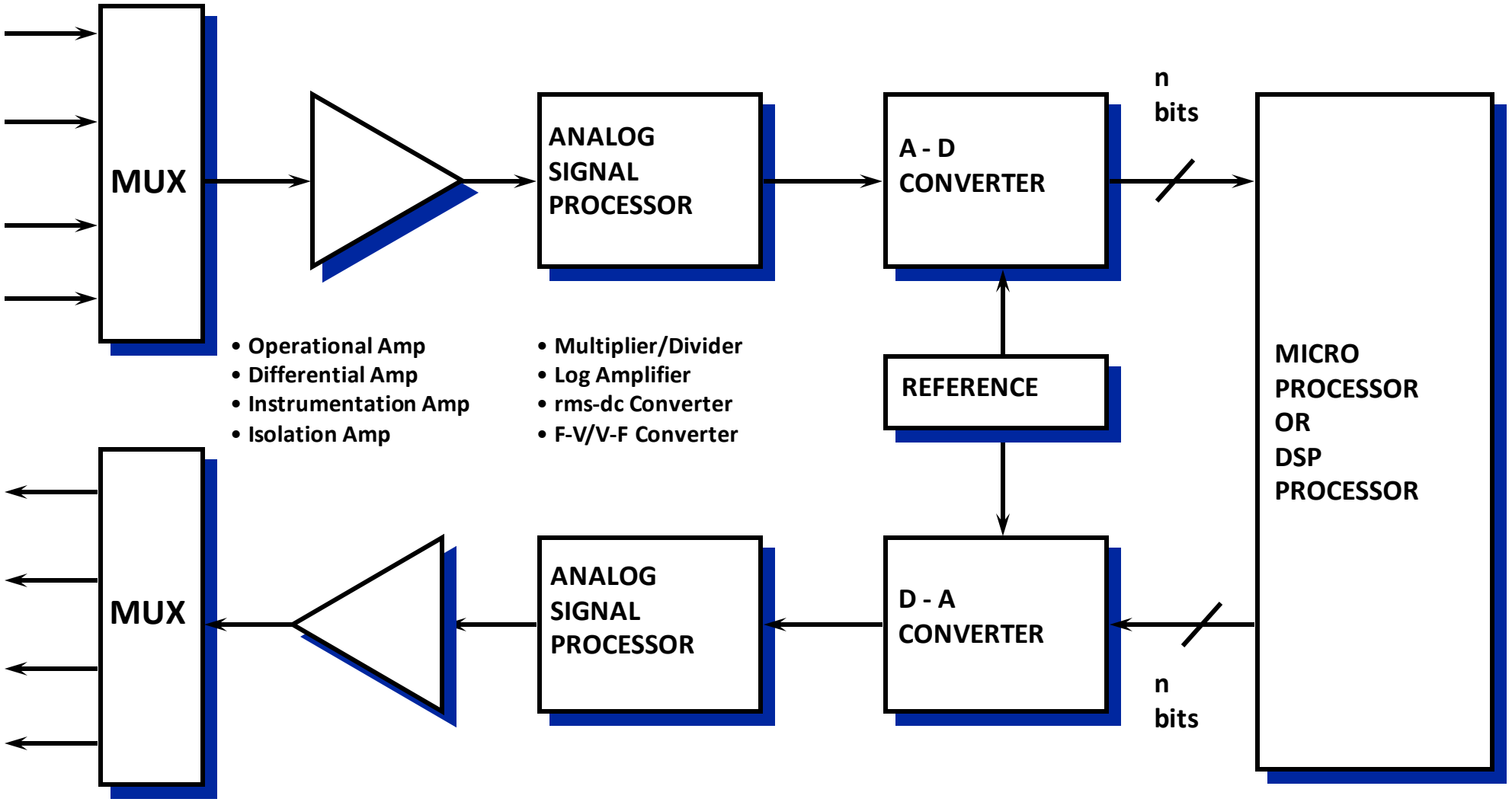
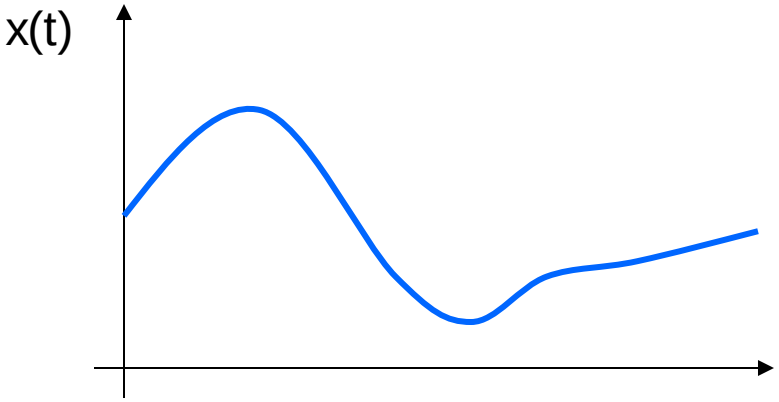
The Measurement and Control Loop



Definition & Necessity

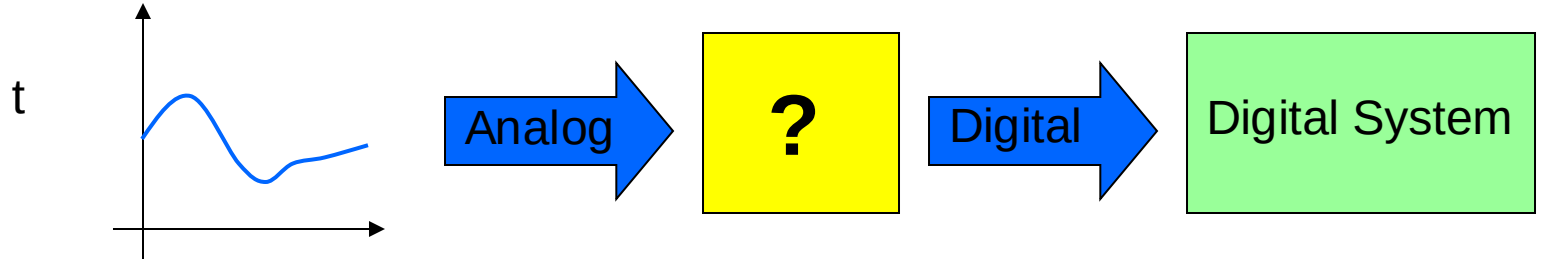
Most signals we want to process are analog

i.e.: they are continuous and can take an inifinity of values



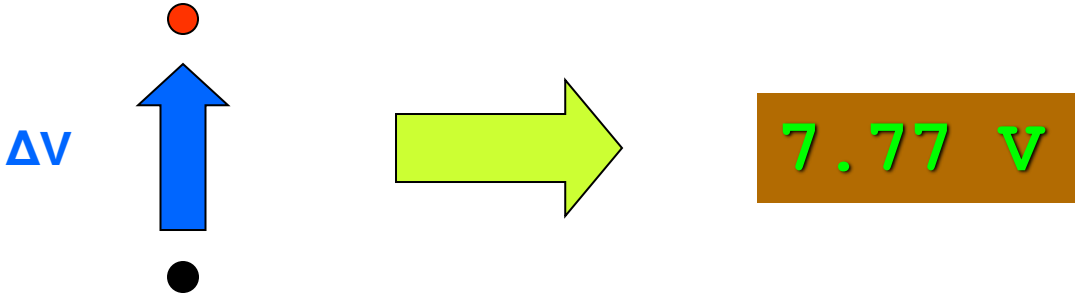
Digital systems require discrete digital data

ADC converts an analog information into a digital information

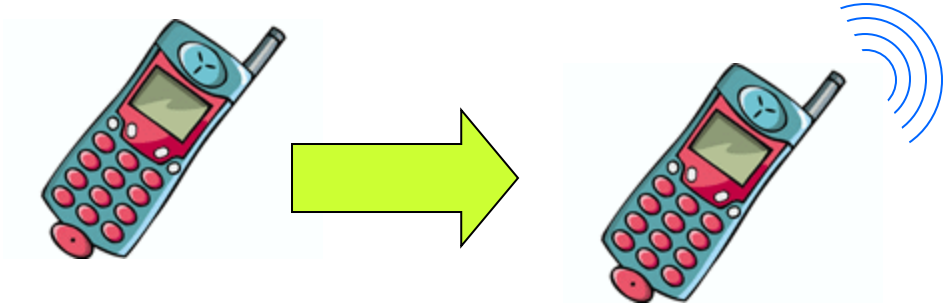


Applications

Voltmeter



- **Cell phone (microphone)**



Analog to Digital Conversion Process

3 steps:

Sampling

Quantification

Coding

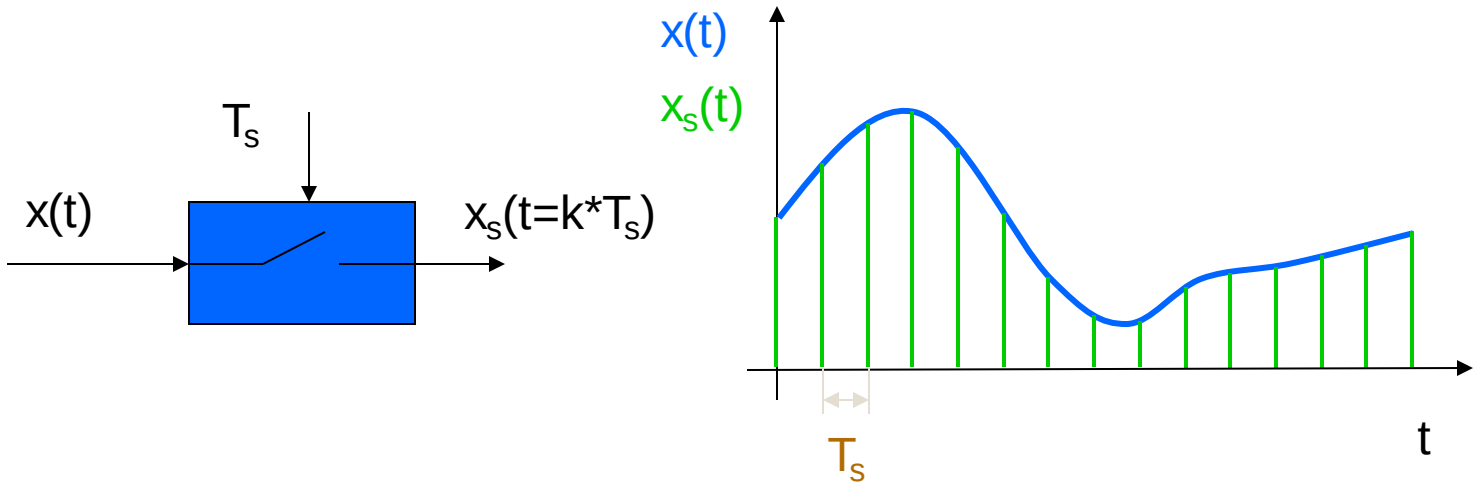
These operations are all performed in a same element:
the A to D Converter

Conversion Process: Sampling

Digital system works with discrete states

The signal is only defined at determined times

The sampling times are proportional to the sampling period (T_s)



Conversion Process: Quantification

The signal can only take determined values

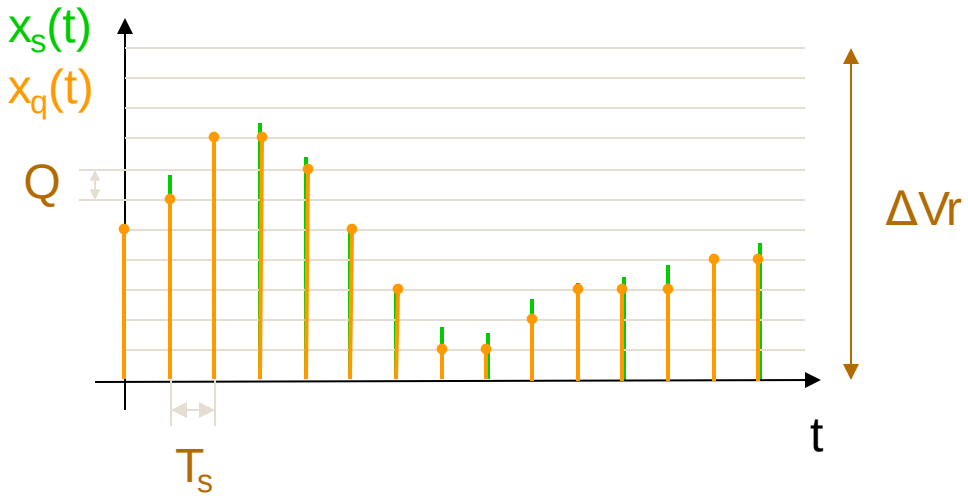
Belonging to a range of conversion (ΔV_r)

Based on number of bit combinations that the converter can output

Number of possible states:

$N=2^n$ where n is number of bits

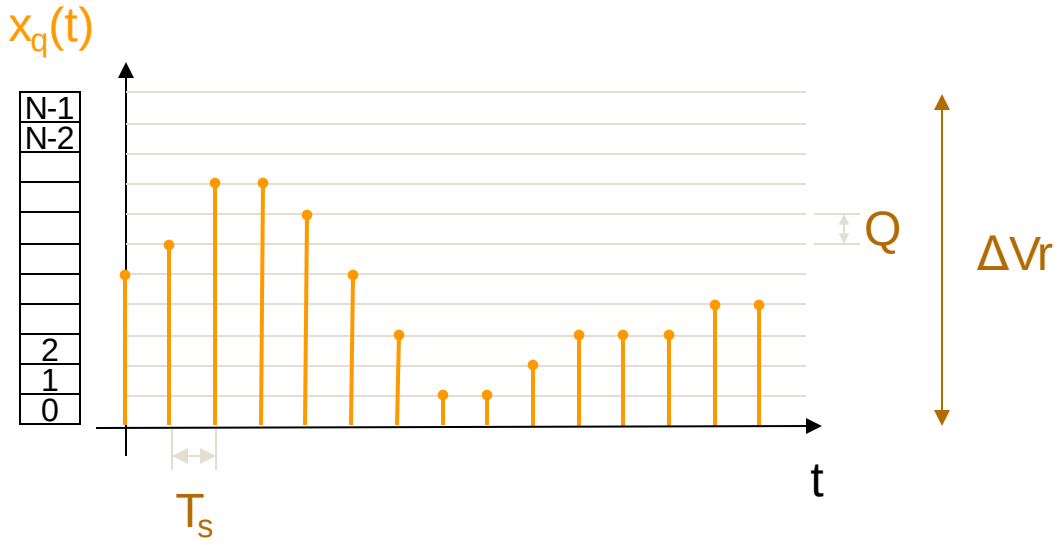
Resolution: $Q= \Delta V_r/N$



Conversion Process: Coding

Assigning a unique digital word to each sample

Matching the digital word to the input signal

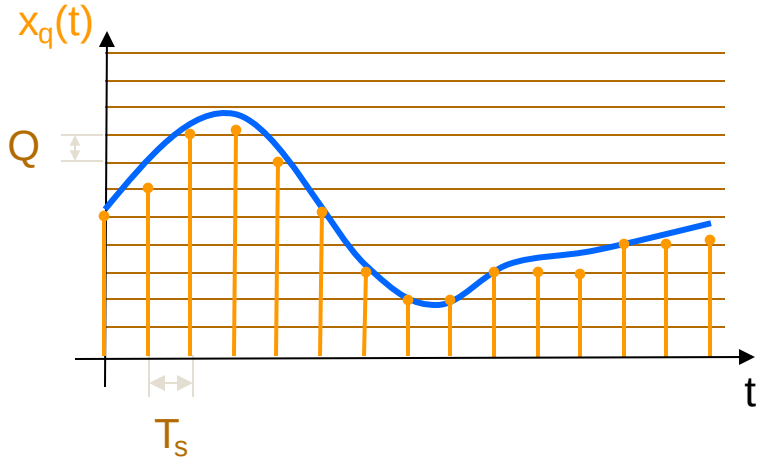


Accuracy in ADC?

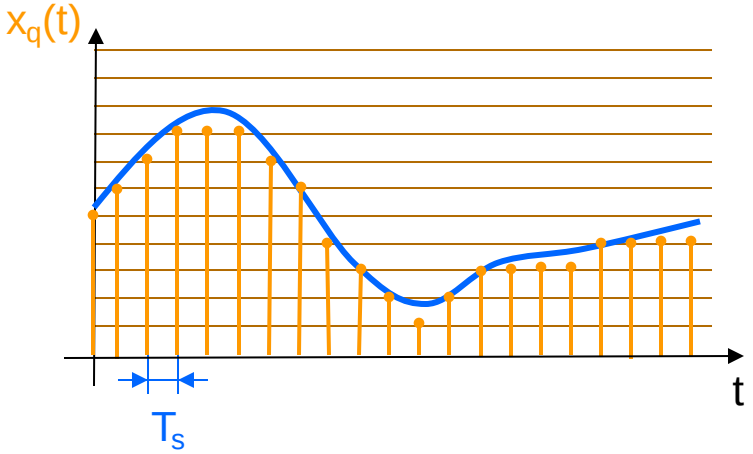
The accuracy of an ADC can be improved by increasing:

- The sampling rate (T_s)
- The resolution (Q)

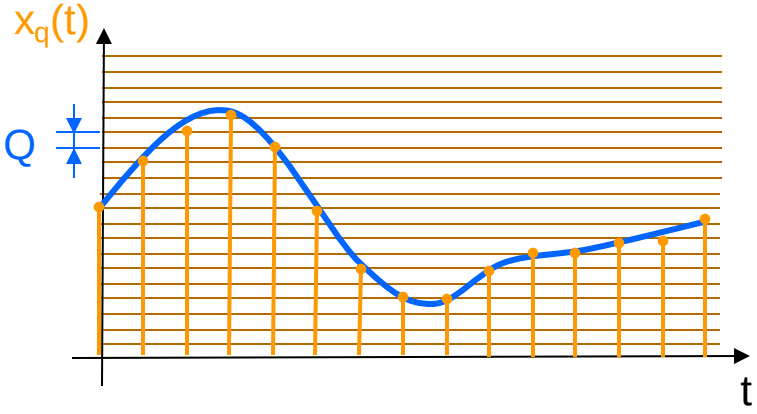
Accuracy in ADC?



Higher Sampling rate



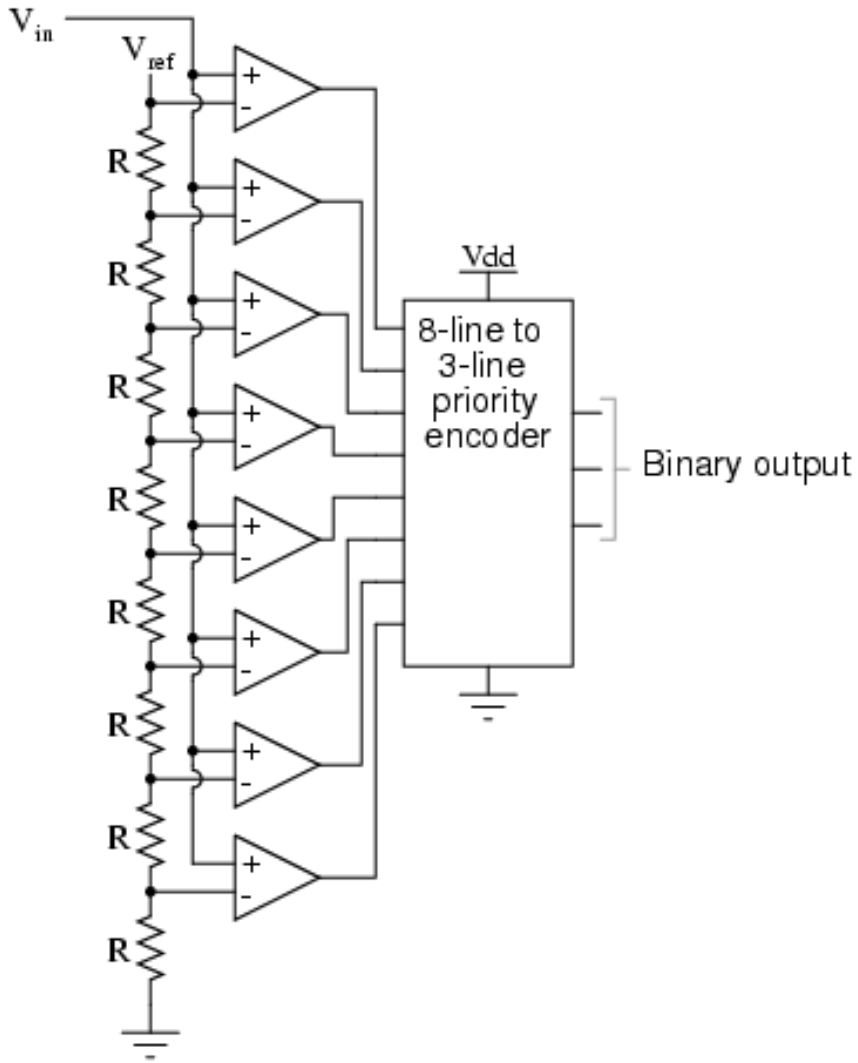
Higher Resolution



Types of ADC

- Flash ADC
- Sigma-delta ADC
- Successive approximation converter

Flash ADC



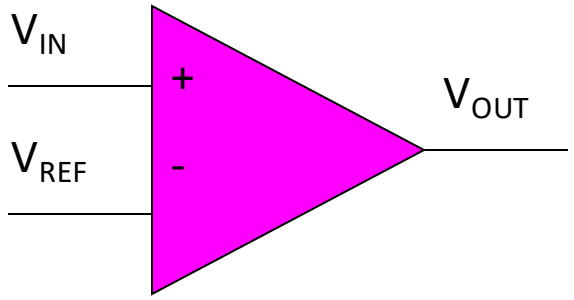
"parallel A/D"

Uses a series of comparators

Each comparator compares V_{in} to a different reference voltage, starting with V_{ref} = 1/2 lsb

Flash ADC

Comparator is one use of an Op-Amp

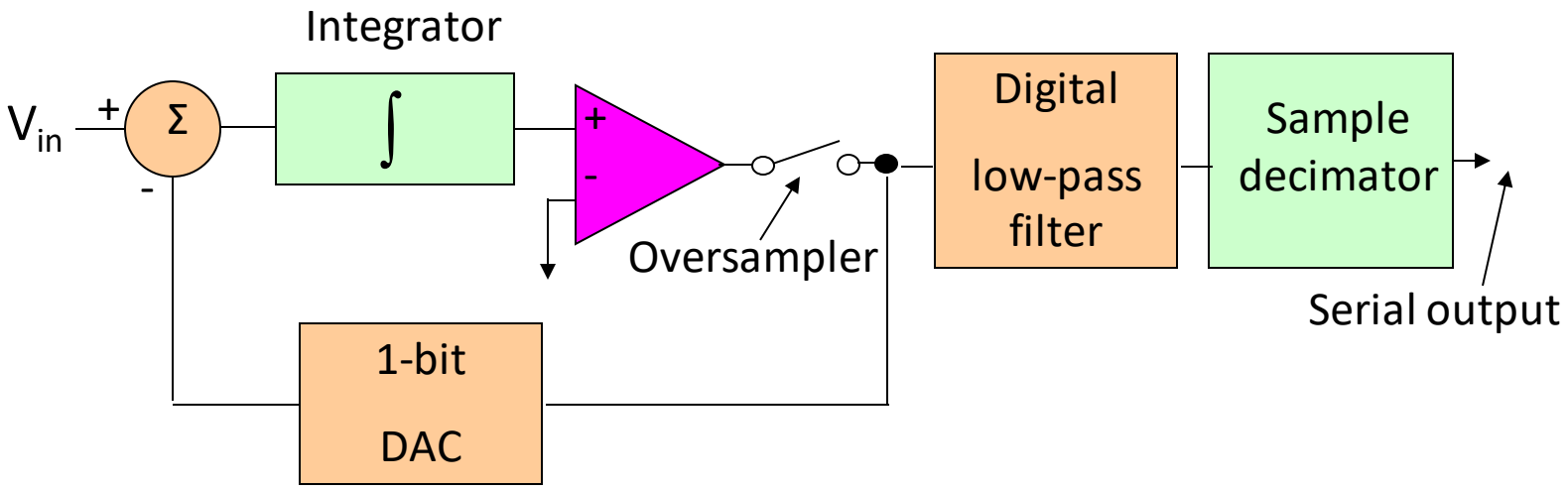


If	Output
$V_{IN} > V_{REF}$	High
$V_{IN} < V_{REF}$	Low

Flash ADC

Advantages	Disadvantages
Very fast	Needs many parts (255 comparators for 8-bit ADC) Lower resolution Expensive Large power consumption

Sigma-Delta ADC



Oversampled input signal goes in the integrator

Output of integration is compared to GND

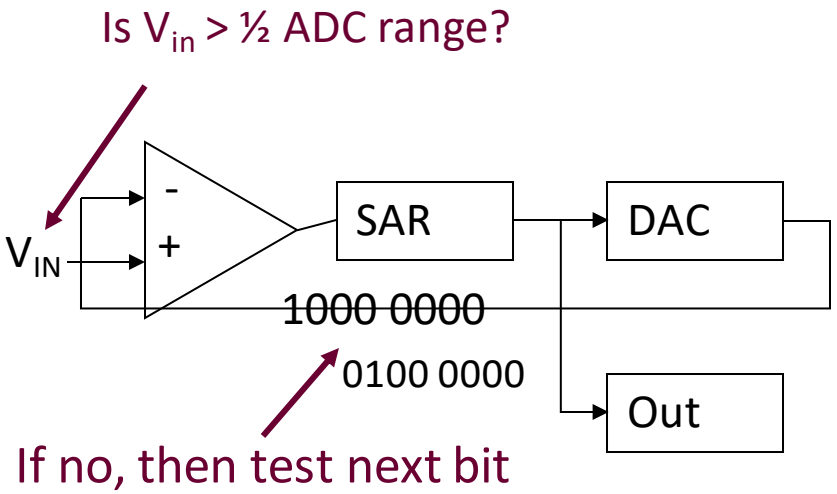
Iterates to produce a serial bitstream

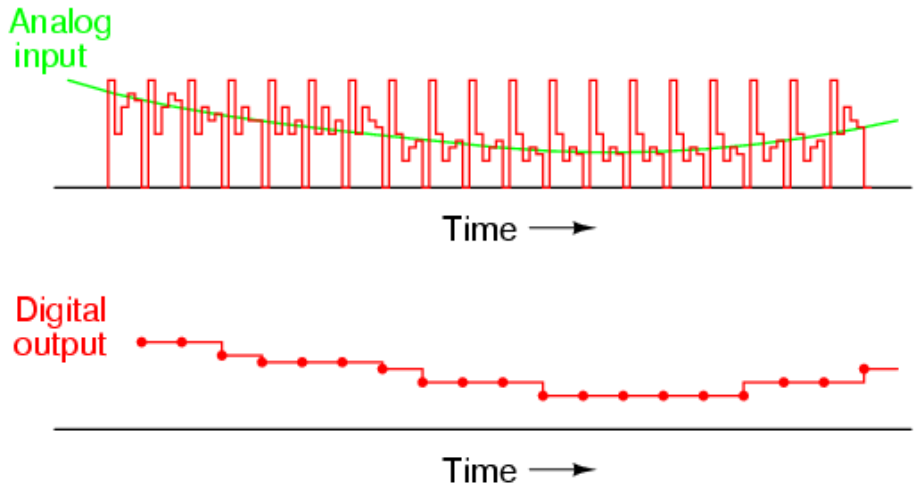
Output is serial bit stream with # of 1's proportional to V_{in}

Sigma-Delta ADC

Advantages	Disadvantages
High resolution No precision external components needed	Slow due to oversampling

Successive Approximation ADC





Sets MSB

Converts MSB to analog using DAC

Compares guess to input

Set bit

Test next bit

Successive Approximation ADC

Advantages

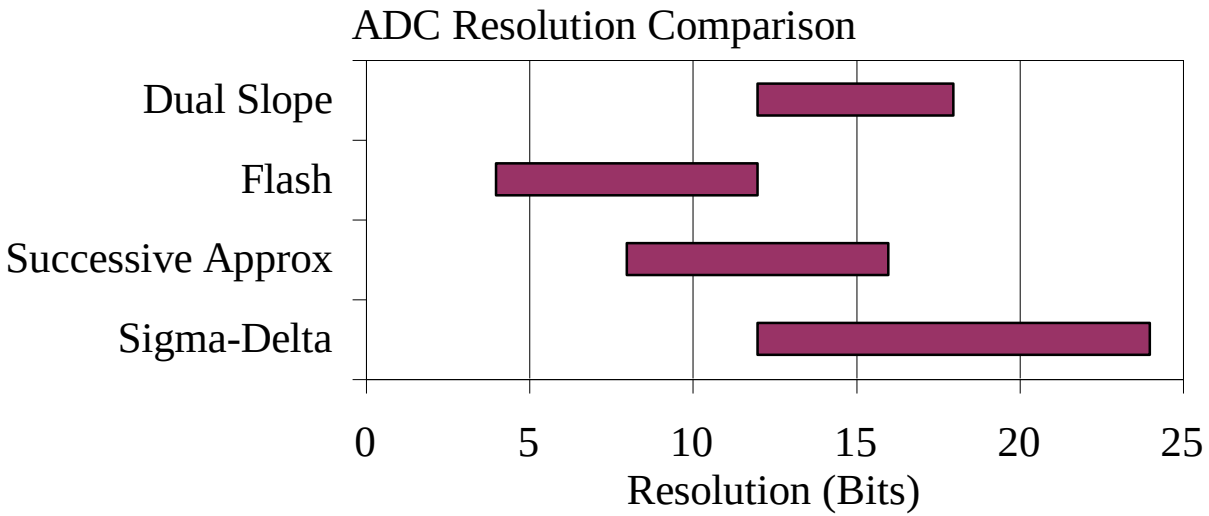
- Capable of high speed
- Medium accuracy compared to other ADC types
- Good tradeoff between speed and cost

Disadvantages

Higher resolution successive approximation ADCs will be slower

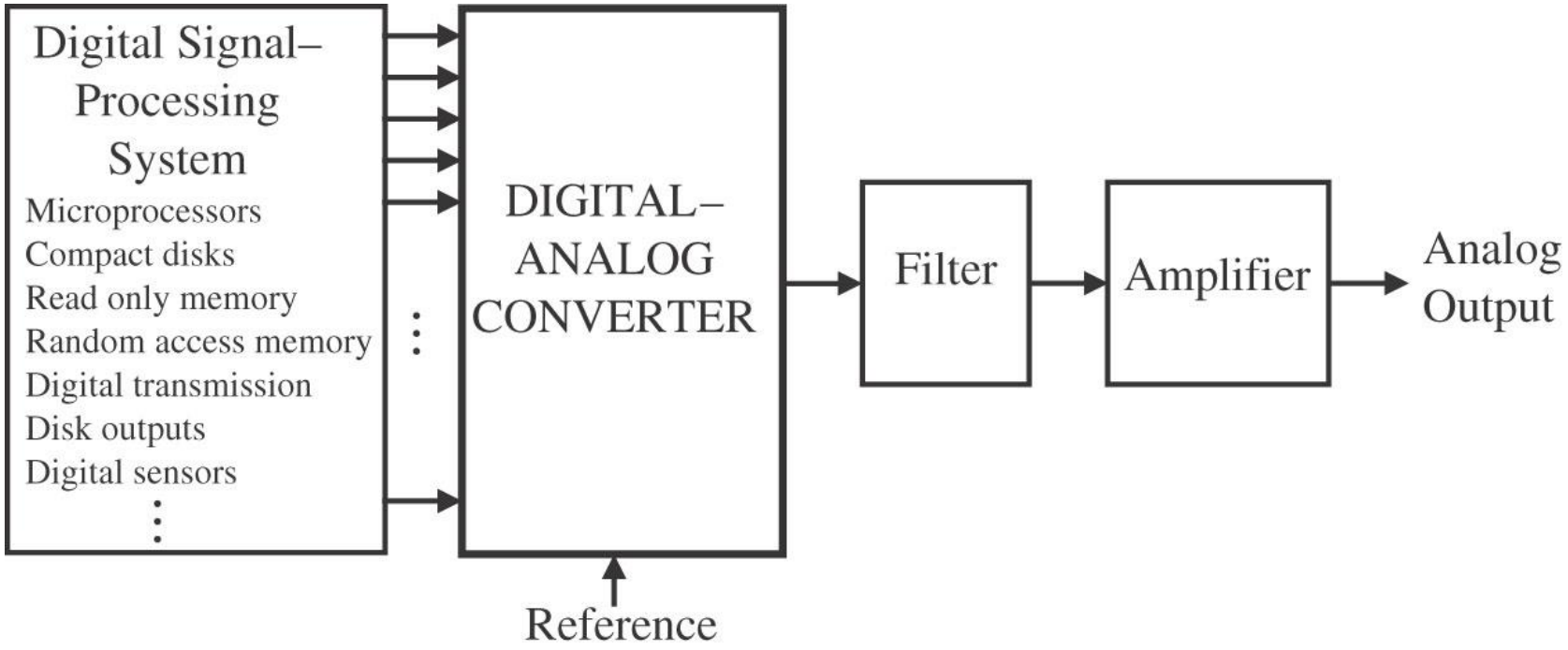
Speed limited ~5Msps

Comparison of ADC Types

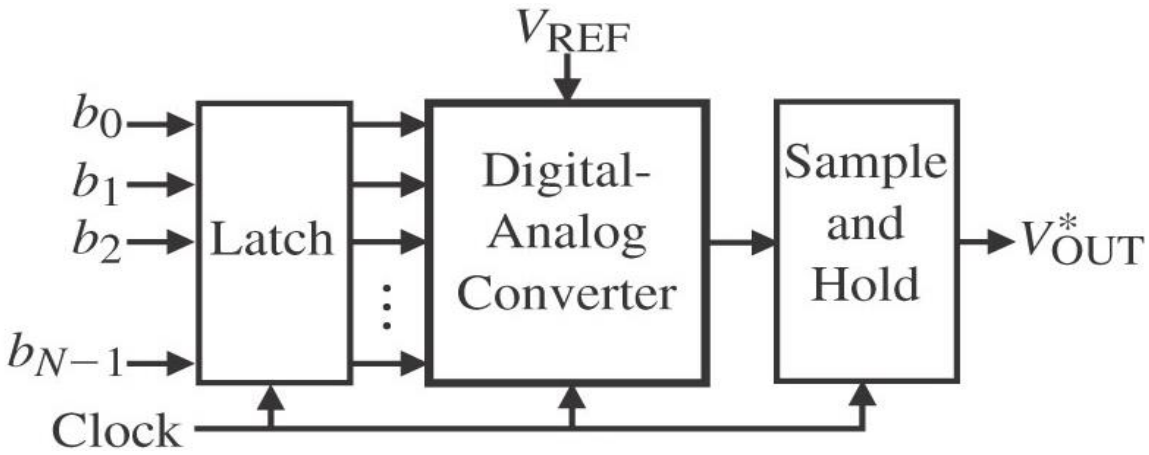


Type	Speed (relative)	Cost (relative)
Dual Slope	Slow	Med
Flash	Very Fast	High
Successive Appox	Medium – Fast	Low
Sigma-Delta	Slow	Low

DAC in signal-processing



Clocked DAC



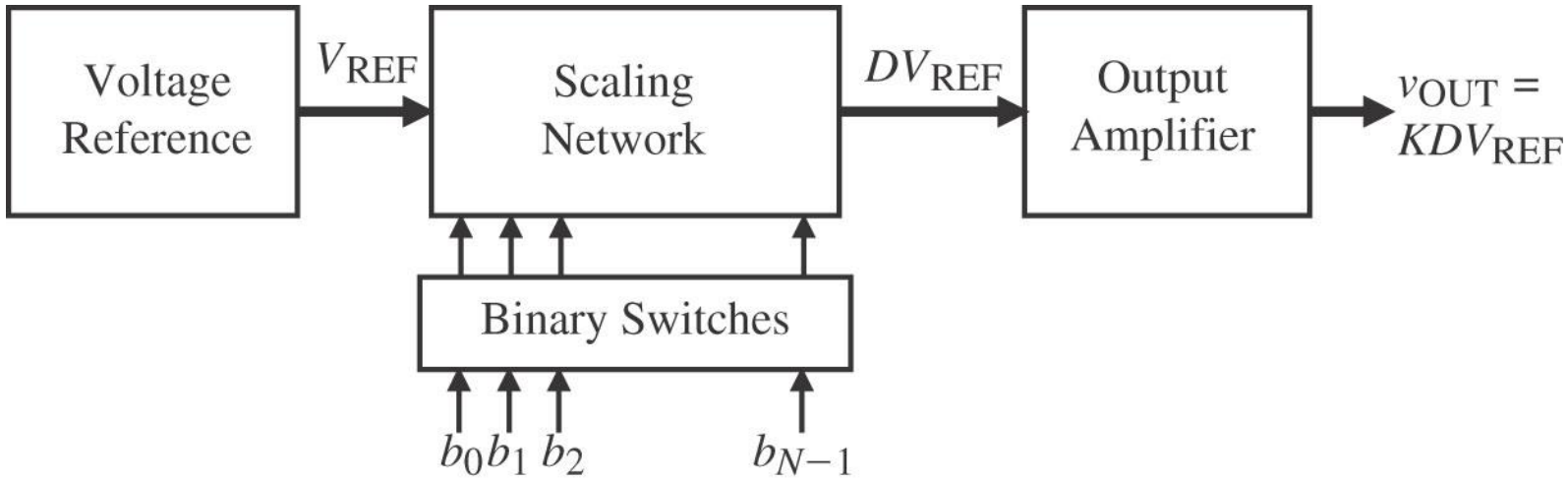
$$V_{OUT} = K.V_{REF}.D$$

$$D = \frac{b_0}{2^1} + \frac{b_1}{2^2} + ... + \frac{b_{N-1}}{2^N}$$

K= Scaling factor
N = No. of bits in digital word

Here, $b_{0.....}b_{N-1}$ will be either 0 or 1 based on the digital word input

DAC Architecture

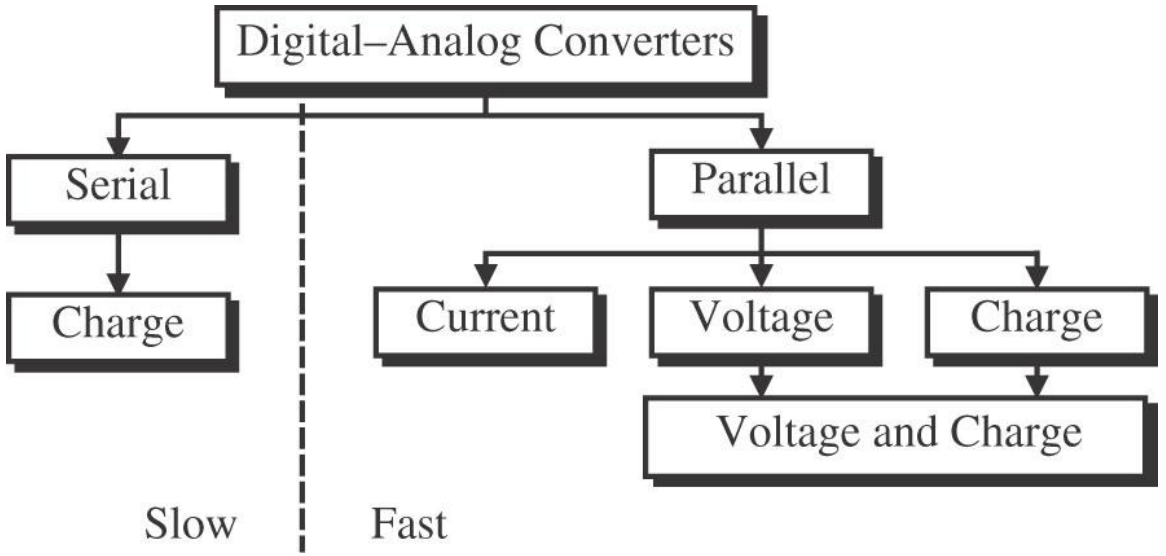


•The general DAC includes binary switches, a scaling network, and an output amplifier.

•The scaling network and binary switches operate on the reference voltage to create a voltage that has been scaled by the digital word.

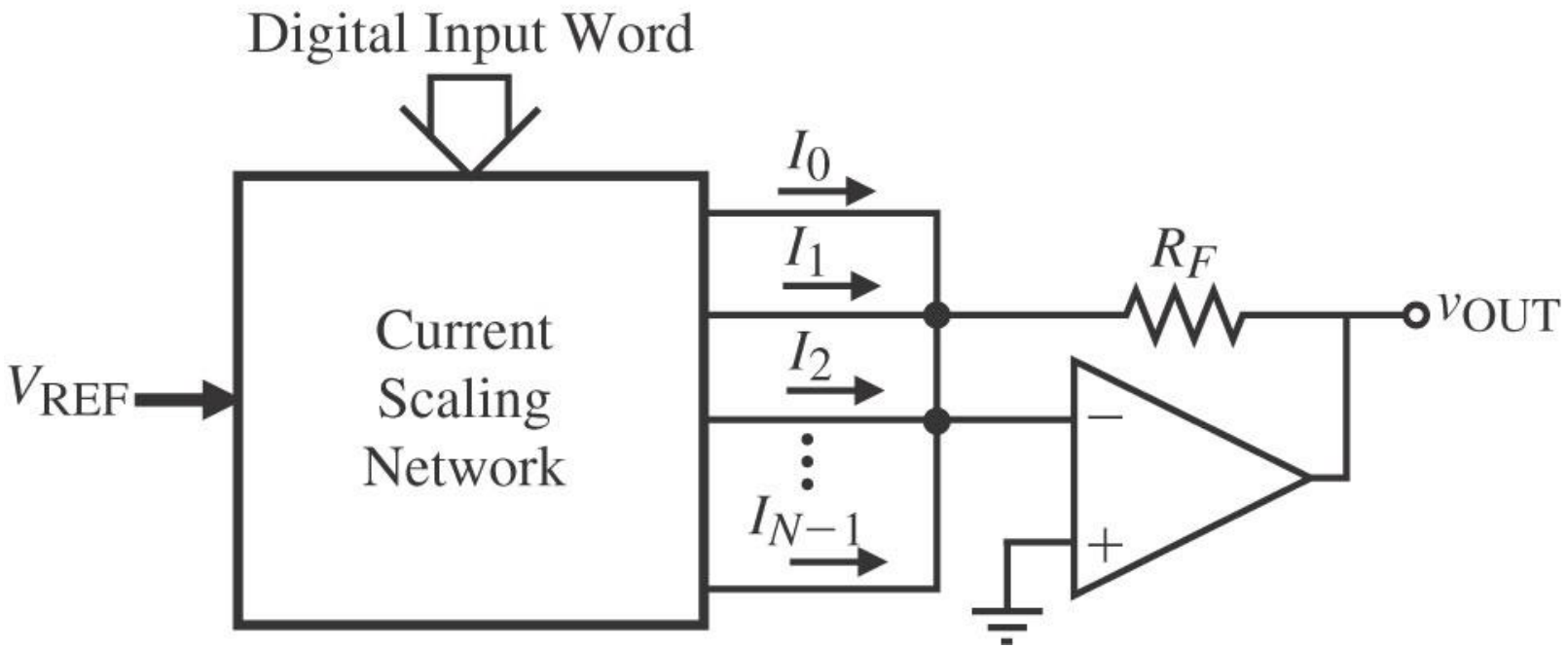
•The scaling mechanism may be voltage, current or charge scaling.

Classification of DACs



- Serial DACs convert one bit at a time. The total conversion time is *NT*, where N is the number of bits and T is the time for conversion of 1-bit.
- Parallel DAC convert all the bits at a time. The total conversion time is *T.*
- Current scaling DACs typically convert the reference voltage, Vref, to a set of binary-weighted current. These currents are generally applied to an op amp in the inverting configuration to create the analog output voltage, V_{out}.

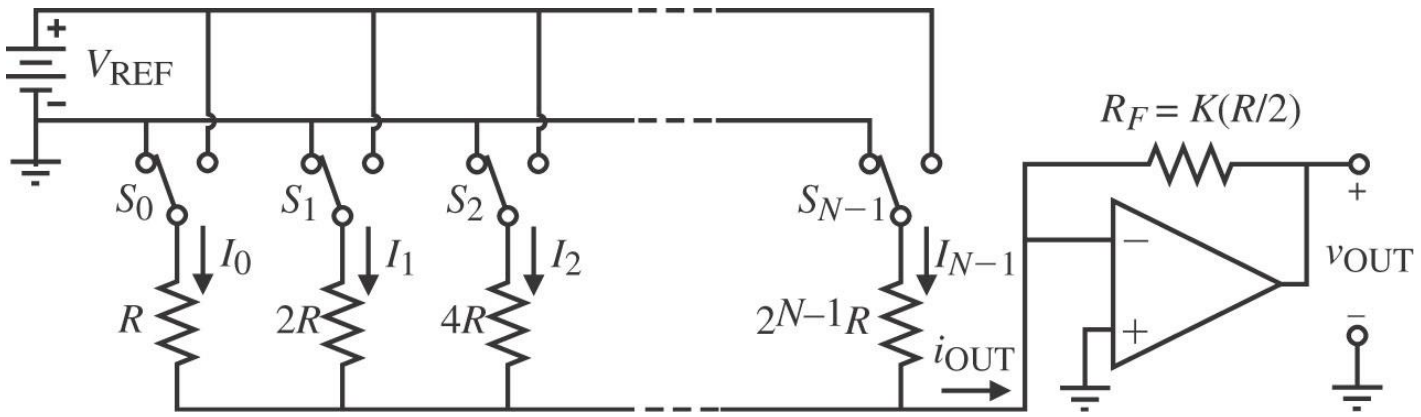
Architecture of Current Scaling DAC



$$V_{OUT} = -R_F\left(I_0 + I_1 + I_2 + \ldots\ldots + I_{N-1}\right)$$

Currents, I_0, I_1, I_2,…, I_{N-1} are binary weighted currents.

Binary-weighted resistor DAC



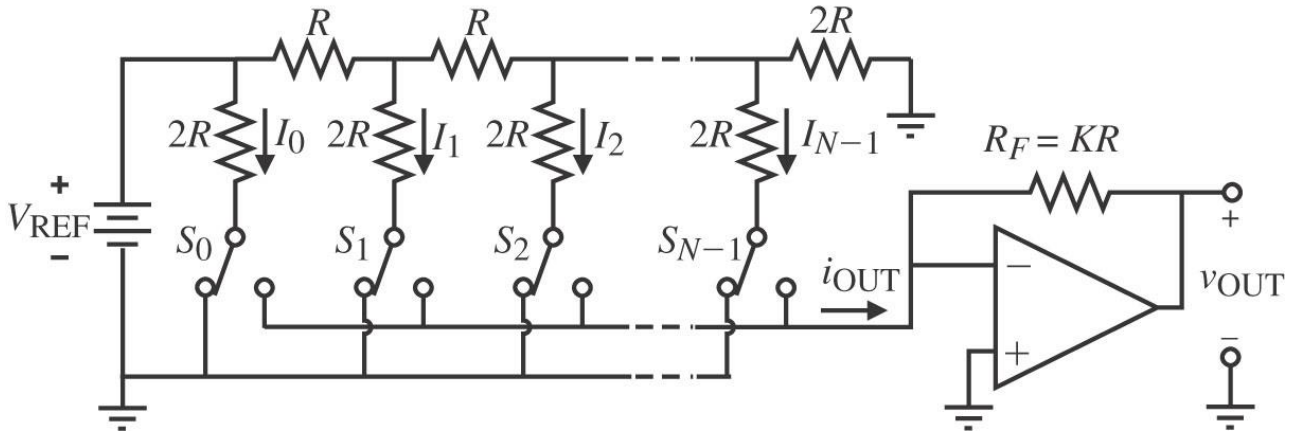
$$v_{OUT} = -R_F i_{OUT} = -\frac{KR}{2}\left(\frac{b_0}{R} + \frac{b_1}{2R} + \frac{b_2}{4R} + \ldots.. + \frac{b_{N-1}}{2^{N-1}R}\right)V_{REF}$$

- The op amp feedback resistor R_F can be used to scale the gain of the DAC.

- Advantage: Insensitive to parasitic capacitors and it therefore fast
- Disadvantage: Require resistors with a large value spread. Chip area becomes high.

- The component value spread can be expressed as $=(1/2^{N-1})$. For N=8, CS = 1/128.
- Large component spread (CS) leads to poorer matching between the various resistors.

R-2R ladder implementation of binary-weighted resistor DAC

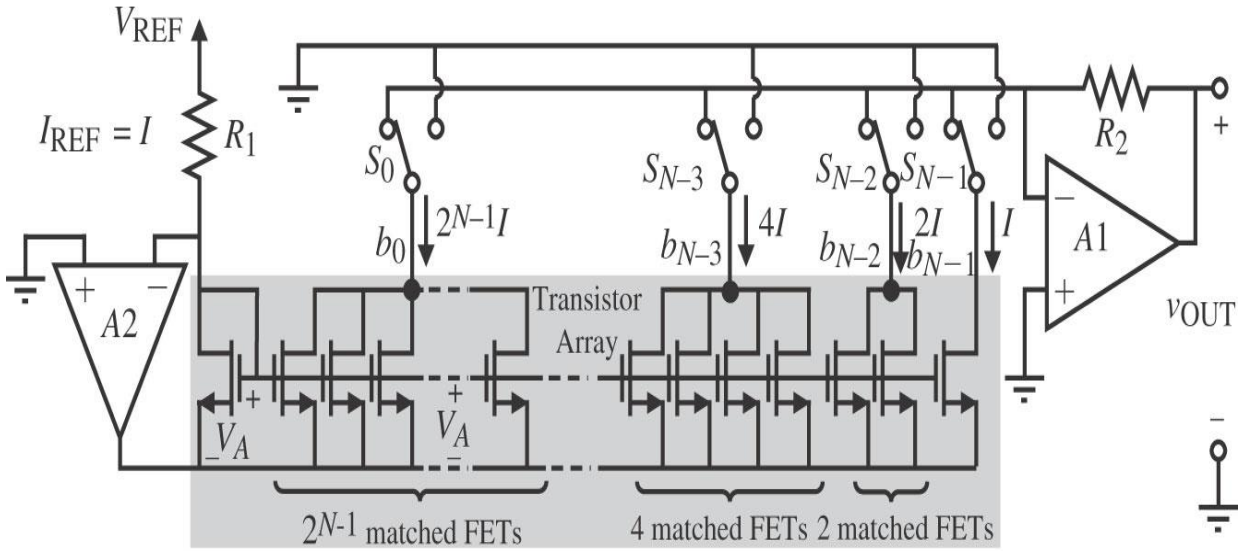


$$I_0 = \frac{V_{REF}}{2R}, I_1 = \frac{V_{REF}}{4R}, I_2 = \frac{V_{REF}}{8R}, ..., I_{N-1} = \frac{V_{REF}}{2^N R}$$

- A resistor of only ONE value can be used to design the whole circuit. **Series** combination of two equal resistors doubles the value. **Parallel** combination of two equal resistors results in half the value.

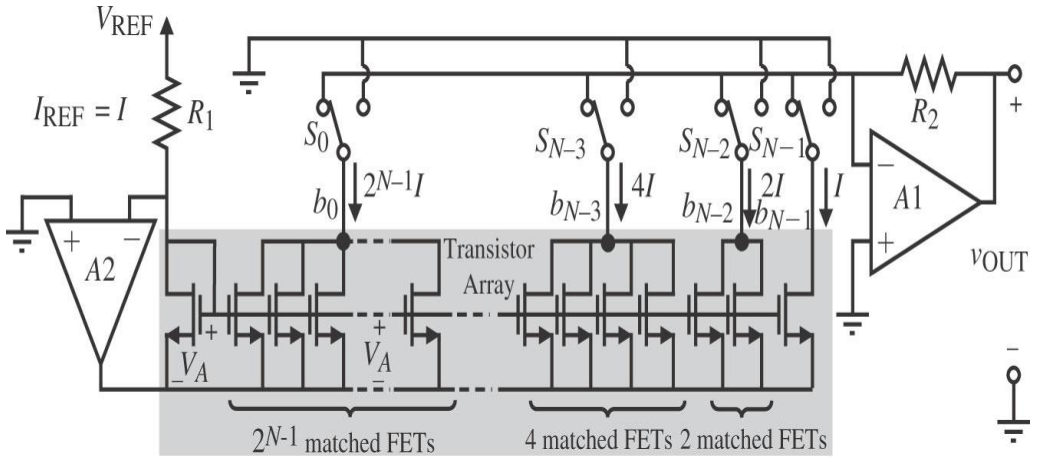
- While, the problem of large spread resistors is eliminated, there are floating nodes in this design.

DAC implementation using matched MOSFETs



- The accuracy of this design depends on the ratio of W/L. Typically this is close to the resistor DAC.
- This design should be limited to N=8, as they will increase overall size dramatically unless the transistor size is really small.
- The reference voltage, V_{REF}, is converted to reference current, I_{REF}. $I_{REF}=V_{REF}/R$.
- The transistors are grouped to form the binary-weighted currents attached to the bottom terminal of the switches S_0, S_1, S_2,….., S_{N-1}.

DAC implementation using matched MOSFETs

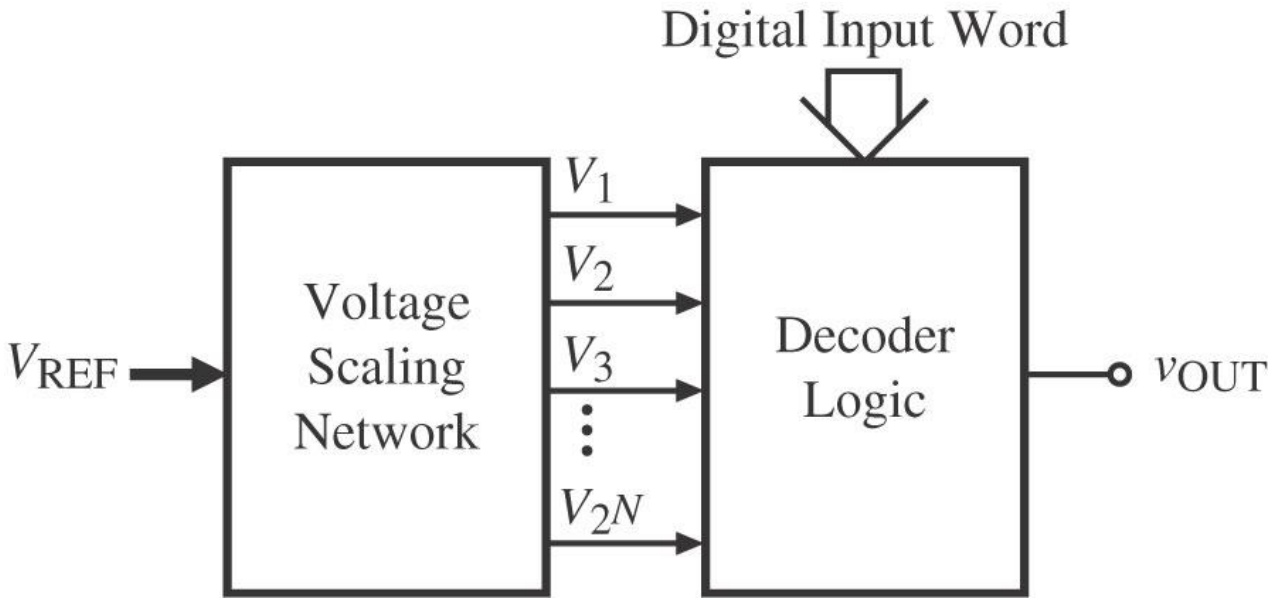


$$v_{OUT} = R_2\left(b_{N-1}.I + b_{N-2}.2I + b_{N-3}.4I + ... + b_0.2^{N-1}I\right)$$

$$If\ I = I_{REF} = \frac{V_{REF}}{2^N R_2}, then$$

$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + ... + \frac{b_{N-3}}{2^{N-2}} + \frac{b_{N-2}}{2^{N-1}} + \frac{b_{N-1}}{2^N}\right)V_{REF}$$

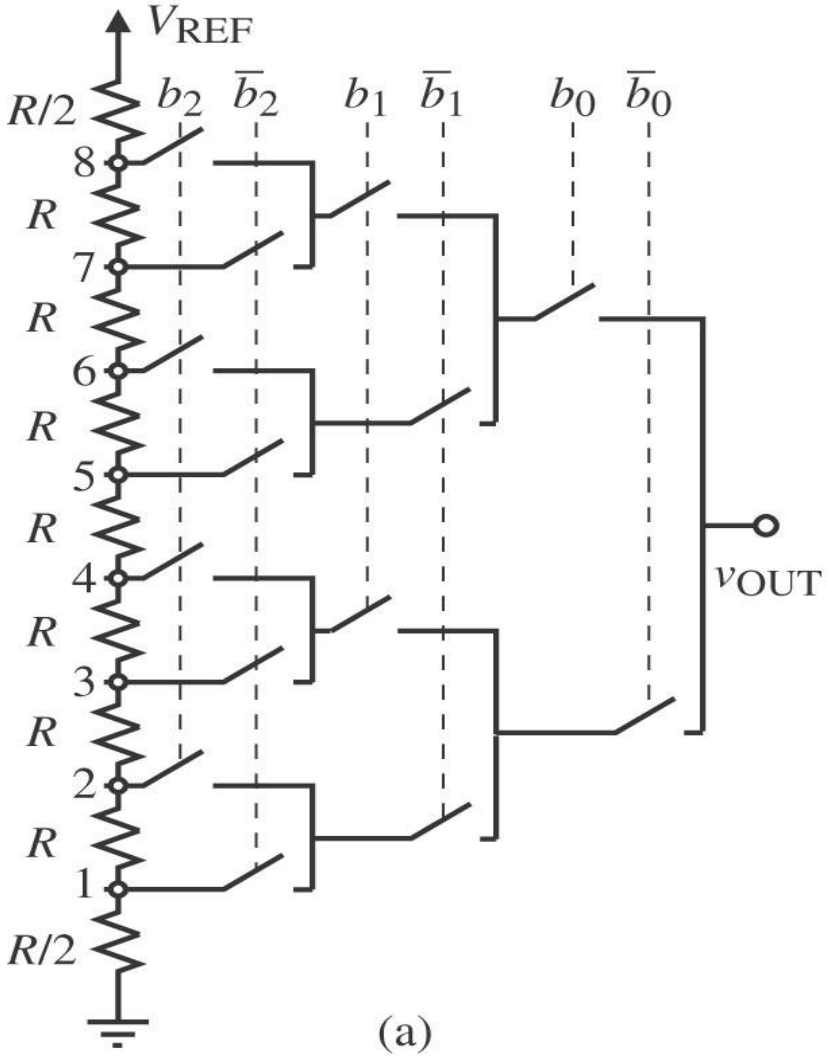
Architecture of Voltage Scaling DAC



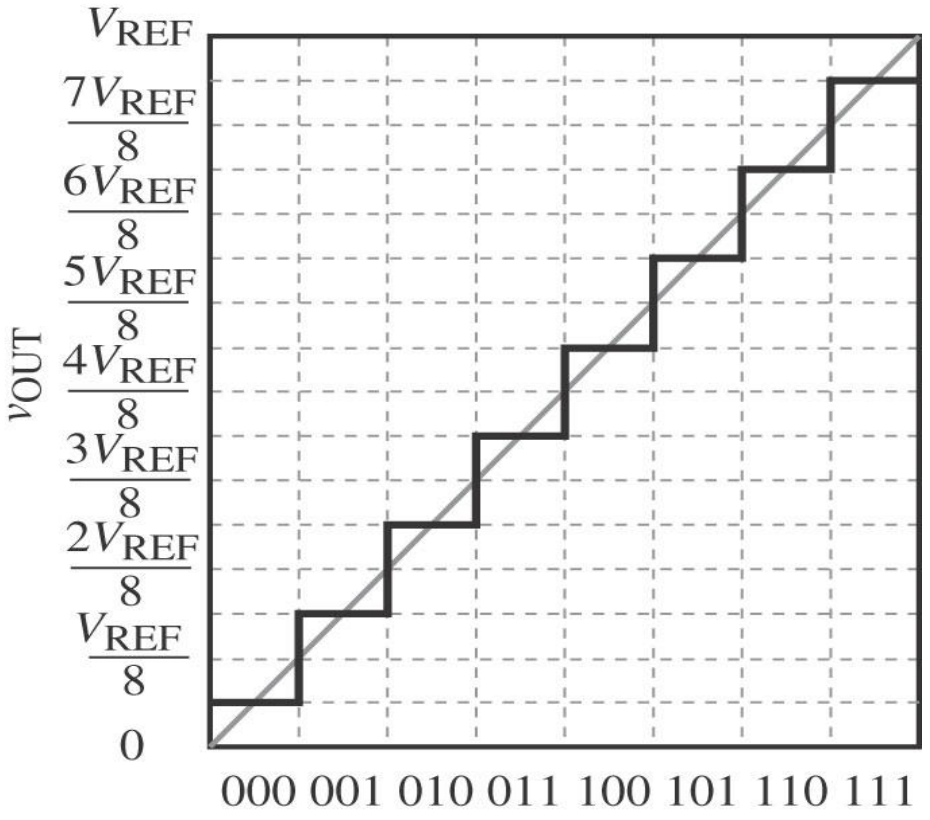
- Voltage scaling network convert the V_{REF} to a set of 2^N voltages that are decoded to a single analog output by the input digital word.

- The Decoder logic simply connects one of the V_1, V_2, V_3,….,$V_2{}^N$ voltages to v_{OUT}.

3-b voltage scaling DAC & I-O characteristics

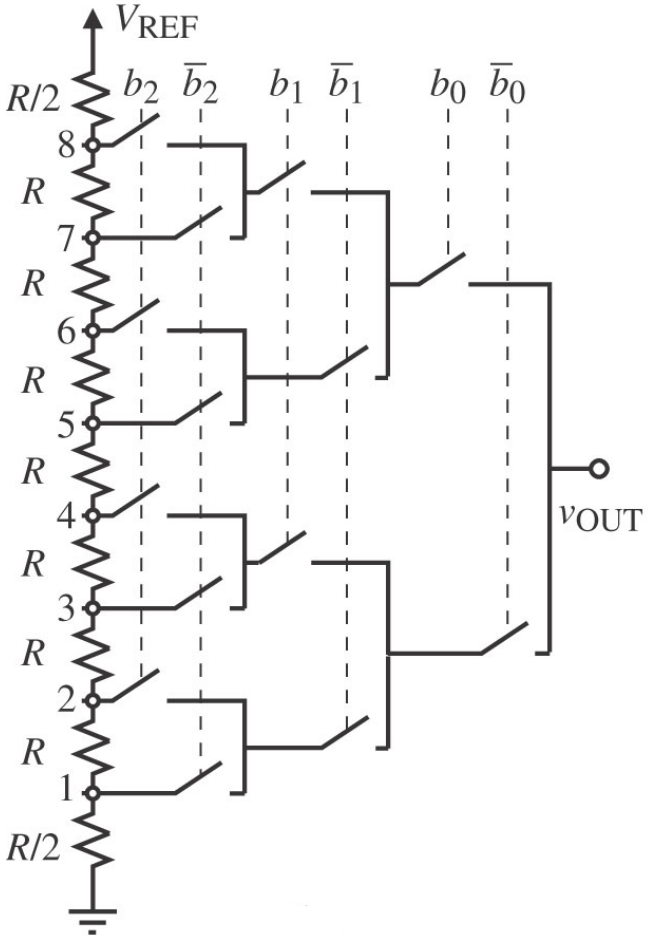


(a)



(b)

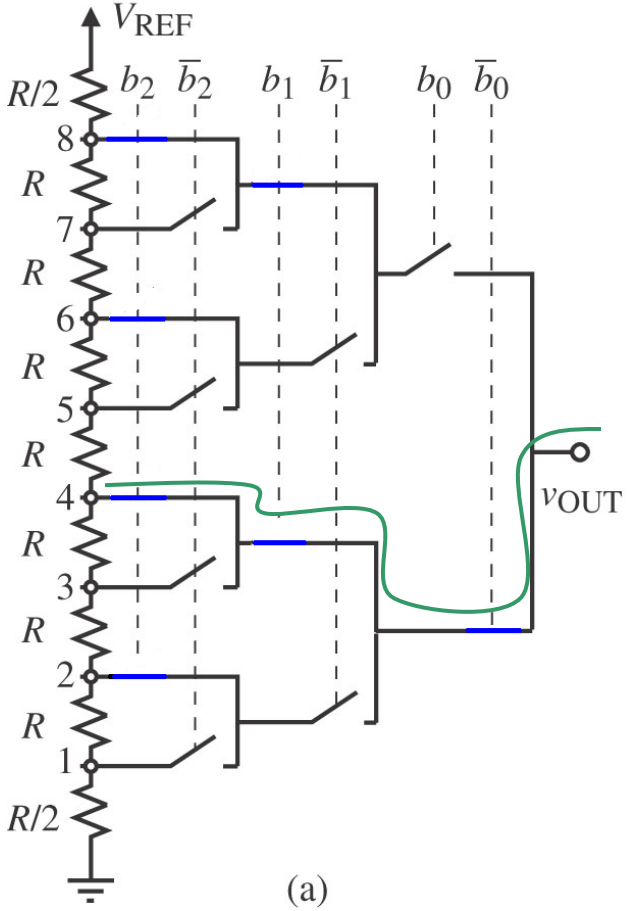
Voltage scaling DAC (cont.,)



Binary word = “110”

v_{OUT} =??

Voltage scaling DAC (cont.,)



(a)

Binary word = "110"

Node 4 is connected to v_{OUT}.

$$v_{OUT} = \left(\frac{3R + \frac{R}{2}}{8R}\right) V_{REF}$$

In general,

$$v_{OUT} = \left(\frac{2n - 1}{16}\right) V_{REF}$$

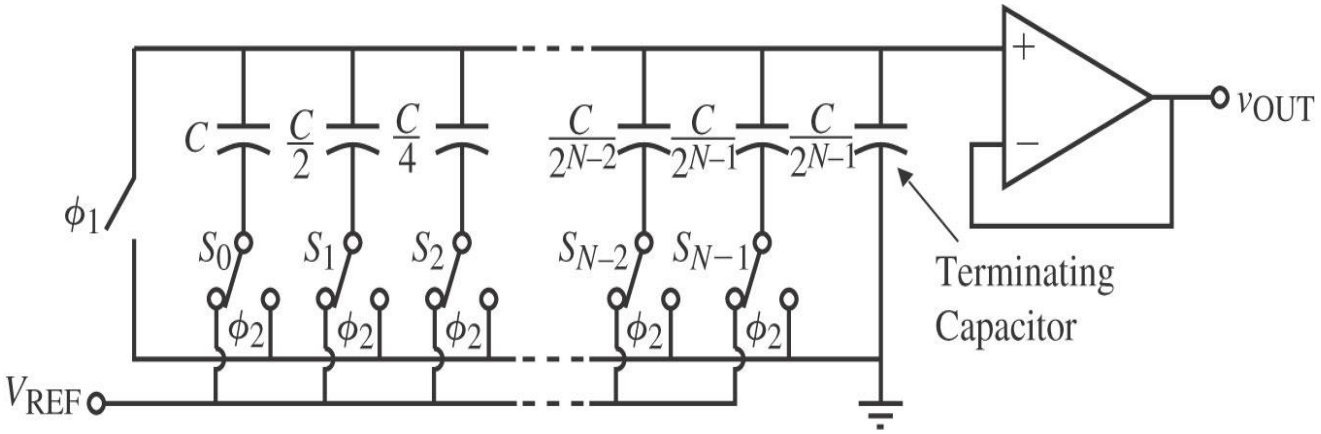
Advantages:

- Faster
- No Decoder is necessary

Disadvantages:

- Resistance in circuit increases, as the switches are connected in series.
- Might have some problem with respect to series channel connections in transistors.

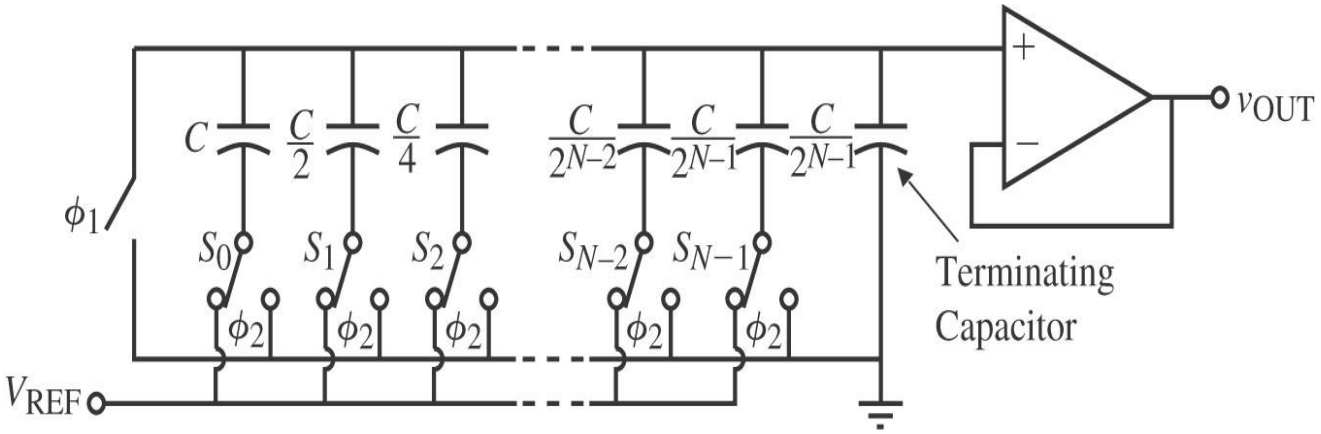
Charge Scaling DAC



- Here, a two-phase non-overlapping cock SHOULD be used for this converter.

- During Φ_1 the top and bottom plates of all the capacitors in the array are grounded. During Φ_2, the capacitors associated with bits that are 1 are connected to V_{REF} and those with bits that are 0 are connected to ground. The output is valid during Φ_2.

Charge Scaling DAC



$$V_{REF}C_{eq} = V_{REF}\left(b_0C + \frac{b_1C}{2} + \frac{b_2C}{2^2} + ... + \frac{b_{N-1}C}{2^{N-1}}\right) = C_{tot}v_{OUT} = 2C.V_{OUT}$$

$$v_{OUT} = \left[b_0 2^{-1} + b_1 2^{-2} + b_2 2^{-3} + ... + b_{N-1}2^{-N}\right] V_{REF}$$

Performance of Parallel DACs

DAC Type	Advantage	Disadvantage
Current Scaling	Fast, insensitive to switch parasitics	Large element spread
Voltage Scaling	Equal resistors	Large area, Sensitive to parasitic capacitance
Charge Scaling	Fast, good accuracy	Large element spread